Please replace the paragraph beginning at page 6, line 4 with the following paragraph:

Figure 9 is one embodiment of a computer system suitable for use with the invention.

Please replace the paragraph beginning at page 12, line 5 with the following paragraph:

Figure 7 is a block diagram illustrating an overview of an IC design simulation tool. As illustrated, IC design simulation tool 700 is constituted with design reader 702, static partitioner 703 and simulation engine 704 comprising dynamic partitioner 707, scheduler 709, node evaluator 708 and model evaluators 706. The elements are operatively coupled to each other as shown. Design reader 702 and some model evaluators 706, in particular a transistor model evaluator and a wire model evaluator, are incorporated with the teachings of the present invention. Certain aspects of static partitioner 703, dynamic partitioner 707 and scheduler 709 are the subject of co-pending U.S. Patent application number 09/333,124, filed June 14, 1999, and entitled "CIRCUIT SIMULATION USING DYNAMIC PARTITION AND ON-DEMAND EVALUATION" which is hereby fully incorporated by reference.

Please replace the paragraph beginning at page 12, line 20 with the following paragraph:

Design reader 702 is used to read design description 710 provided by a designer. Design description 710 includes connectivity information connecting various models modeling electronic devices in the IC design. In one embodiment, in addition to flattening a hierarchical design, design reader 702, also assigns device characterizations to selected ones of the electronic devices of the IC design. In one embodiment the device characterizations are determined as described above. Static partitioner 703 pre-compiles or pre-partitions the IC design into static partitions as well as pre-processes the static partitions into a form particularly suitable for the dynamic partitioner 707.

Please replace the paragraph beginning at page 13, line 5 with the following paragraph:

During simulation, dynamic partitioner 707 further forms and re-forms dynamic partitions of the IC design that are relevant, referencing the pre-formed static partitions. Scheduler 709 determines whether evaluations are necessary for the dynamic partitions for the particular simulation time step, and schedules the dynamic partitions for evaluation on an as-needed or on-demand basis. Accordingly, node evaluator 708 and model evaluators 706 are selectively invoked on an as-needed or on-demand basis to evaluate the states of the connections connecting the models, and various parameter values of the models, such as current, voltage and so forth, respectively.

Please replace the paragraph beginning at page 14, line 1 with the following paragraph:

Figure 8 is a block diagram illustrating one embodiment of a parasitic extraction tool suitable for use with the present invention. As illustrated, the present invention includes parasitic extraction

tool (PEX) 802 and parasitic database (PDB) 804. PEX 802 generates electrical modeling data for layout nets of an IC design, e.g. a deep sub-micron IC design, and stores the generated electrical modeling data in PDB 804 for use by client applications, such as post layout analysis applications 818. Examples of post-layout analysis applications 818 include Delay Calculator by Ultima Technology of Sunnyvale, CA, and Path Mill and Time Mill by Synopsis Inc. of Mountain View, CA.

Please replace the paragraph beginning at page 14, line 9 with the following paragraph:

PEX 802 generates the electrical modeling data for the layout nets using extracted connectivity and geometrical data of the layout nets. In one embodiment PEX 802 generates capacitive modeling data as described above. As shown, PEX 802 includes read function 806 that operates to input these connectivity and geometrical data of the layout nets. For the illustrated embodiment, the extracted connectivity and geometrical data of the layout nets are input from filtered databases (FDB) 816.

Please replace the paragraph beginning at page 14, line 15 with the following paragraph:

The extracted connectivity and geometrical data are stored in FDB 816 by layout cell hierarchies, one FDB per layout cell hierarchy, and indexed by layout nets. The connectivity and geometrical data were extracted at least in part in accordance with specified parasitic effect windows of the various layers of the IC design. Read function 806 operates to retrieve the connectivity and geometrical data of the layout nets from FDB 816 using the stored layout net indices. FDB 816 is the subject of co-pending U.S. Patent application number 09/052,895, filed March 31, 1998, and entitled "METHOD AND APPARATUS FOR EXTRACTING AND STORING CONNECTIVITY AND GEOMETRICAL DATA FOR A DEEP SUB-MICRON INTEGRATED CIRCUIT DESIGN," which is assigned to the corporate assignee of the present invention. The co-pending application is hereby fully incorporated by reference.

Please replace the paragraph beginning at page 15, line 3 with the following paragraph:

PDB 804 is designed to accommodate a large volume of electrical modeling data and concurrent accesses by multiple client applications, which is typically of today's and future deep sub-micron IC designs and design environments. For the illustrated embodiment, PDB 804 has physical organization 814 that allows a large volume of electrical modeling data to be stored in multiple physical media, and application interface 810 that shields physical organization 814 from PDB users, e.g. PEX 802 and post layout analysis applications 818. Additionally, PDB 802 has logical organization 812 that abstracts physical organization 814 to facilitate implementation of application interface 810.

Please replace the paragraph beginning at page 15, line 12 with the following paragraph:

For the illustrated embodiment, PEX 802 includes write function 808 that operates to store the generated electrical modeling data of the layout nets into PDB 804 using application interface 810. In alternate embodiments, write function 808 may store the generated electrical modeling data of the layout nets using either logical and/or physical organizations 812-814. Similarly, selected ones of the client applications, e.g. post-layout analysis applications 818, may also elect to access PDB 804 through logical and/or physical organizations 812-814.

Please replace the paragraph beginning at page 15, line 19 with the following paragraph:

Read function 806 and write function 808 are the subject of co-pending U.S. Patent application number 09/052,915, filed March 31, 1998 and entitled "METHOD AND APARATUS FOR GENERATING AND MAINTAINING ELECTRICAL MODELING DATA FOR A DEEP SUB-MICRON INTEGRATED CIRCUIT DESIGN," which is assigned to the corporate assignee of the present invention. The co-pending application is hereby fully incorporated by reference. Except for read function 806 and write function 808, PEX 802 is intended to represent a broad category of electrical modeling tools known in the art. Examples of these electrical modeling tools include but not limited to Pattern Engine of xCalibre by Mentor Graphics, Columbus by Frequency Technology of San Jose, CA, and Arcadia by Synopsis.

Please replace the paragraph beginning at page 16, line 6 with the following paragraph:

Figure 9 is one embodiment of a computer system suitable for use with the invention. Computer system 900 can be used, for example, for extraction and/or modeling of integrated circuits using the teachings of the present invention. Computer system 900 includes bus 901 or other communication device to communicate information and processor 902 coupled to bus 901 to process information. While computer system 900 is illustrated with a single processor, computer system 900 can include multiple processors and/or co-processors. Computer system 900 further includes random access memory (RAM) or other dynamic storage device 904 (referred to as main memory), coupled to bus 901 to store information and instructions to be executed by processor 902. Main memory 904 also can be used to store temporary variables or other intermediate information during execution of instructions by processor 902.

Please replace the paragraph beginning at page 16, line 17 with the following paragraph:

Computer system 900 also includes read only memory (ROM) and/or other static storage device 906 coupled to bus 901 to store static information and instructions for processor 902. Data storage device 907 is coupled to bus 901 to store information and instructions. Data storage device 907 such as a magnetic disk or optical disc and corresponding drive can be coupled to computer system 900.

Please replace the paragraph beginning at page 16, line 22 with the following paragraph:

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Computer system 900 can also be coupled via bus 901 to display device 921, such as a cathode ray tube (CRT) or liquid crystal display (LCD), to display information to a computer user. Alphanumeric input device 922, including alphanumeric and other keys, is typically coupled to bus 901 to communicate information and command selections to processor 902. Another type of user input device is cursor control 923, such as a mouse, a trackball, or cursor direction keys to communicate direction information and command selections to processor 902 and to control cursor movement on display 921.

Please replace the paragraph beginning at page 17, line 6 with the following paragraph:

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According to one embodiment, extraction and/or modeling can be performed by computer system 900 in response to processor 902 executing sequences of instructions contained in main memory 904. Instructions are provided to main memory 904 from a storage device, such as magnetic disk, a read-only memory (ROM) integrated circuit (IC), CD-ROM, DVD, via a remote connection (e.g., over a network), etc. In alternative embodiments, hard-wired circuitry can be used in place of or in combination with software instructions to implement the present invention. Thus, the present invention is not limited to any specific combination of hardware circuitry and software instructions.

REMARKS

Reconsideration of the application is respectfully requested in view of the foregoing amendments and following remarks. Claims 15-57 are pending in the application. Claims 15, 35, 47, and 51 are independent. No claims have been allowed.

Cited Art

U.S. Patent No. 6,414,498 to Chen ("Chen") entitled, "System, IC Chip, On-Chip Test Structure, and Corresponding Method for Modeling One or More Target Interconnect Capacitances."

Drawings

The drawings are objected to as failing to comply with 37 CFR 1.84(e), (g), (i) and (p). As indicated in the attached Request for Approval of Revised Drawings, a complete set of revised formal drawings have been submitted for approval that respond to all the above-referenced objections.